REMARKS

The Examiner rejected claims 13-18 under 35 USC 102(b) as being anticipated by Pedder et al. Consideration of claims 1-12 was withheld due to a restriction requirement.

In response to the Examiners action, Applicant has amended claim 13, and added claims 19-29. Claim 13 has been amended to include the limitations of comprising "...**a patterned metal pad disposed on the dielectric layer;**" and "...**solder disposed on the patterned metal pad.**"

These additional limitations find support throughout the present specification. For example, the metal pad is discussed in reference to Figs 2A and 2b on pages 9 and 10 of the specification. Lines 1-2 of page 12 describe that the metal pads can be used as electrical contacts for an optoelectronic device. Support for the solder limitation may be found on page 9 lines 5-6.

The UK patent to Pedder et al. does not teach or disclose the combination claimed in amended claim 13. Metal layer 32 in Pedder et al. is used ONLY as a mask to pattern other layers (e.g. SiO2 layer 30); metal layer 32 is NOT present in the final device, and is not used as a solder pad/electrical contact. Hence, the method and device of Pedder et al. would not function as intended if solder were disposed on the metal layer 32. Instead, Pedder et al. teach that a separate 'wettable metal' (page 8) remains AFTER the metal layer 32 and SiO2 are etched away. The wettable metal (presumably referred to as the 'deposited layer 60' on page 8) is used as an electrical contact for electrical components.

Deposited layer 60 of Pedder et al. is distinct from the patterned metal layer or patterned metal pad in claim 13.

This is because the patterned metal layer and pad of claim 13 are disposed on a dielectric layer. Also, the patterned metal layer and pad serve the dual functions of a solder pad and mask for defining the etched pit.

Hence, claim 13 includes the novel and unobvious combination of the solder disposed on the patterned metal on the dielectric. The device of Pedder et al. cannot have solder or an optoelectronic device on the metal layer 32 that is on top of the SiO2 layer 30.

Claim 19 finds support in Fig. 7 and corresponding description in the present application.

Claim 20 finds support in Figs 8a-8f and corresponding description in the present application.

Claim 21 includes the limitation of an optoelectronic device soldered to the patterned metal pad. This is different from Pedder et al. for the same reasons outlined above. In Pedder et al., an optoelectronic device is soldered to a 'wettable metal' which is deposited directly on the substrate. This limitation finds support on page 9, lines 5-6.

Claim 22 includes the limitation that the patterned metal pad is spaced away from the dielectric sidewall. This limitation is supported by Figs. 1 and 2H and corresponding description.

Claim 23 includes the limitation that the patterned metal layer and patterned metal pad are made of identical deposited materials. This limitation finds support in the specification in lines 32-34, page 9, where the pads and patterned metal layer are described as formed from the same deposited parent material.

Claims 25, 26, 28 and 29 are duplicates of originally filed dependent claims 14 and 16.

Claim 24 is supported by Fig. 7 and corresponding description, and by the original claim 13.

Claim 27 is supported by lines 5-6 on page 9, and by the original claim 13.

In view of the above arguments, applicant respectfully requests allowance of claims 13-29.

Respectfully submitted,

Dan Steinberg
Reg. No. 45,129
Haleos, Inc.
3150 State Street
Blacksburg, VA, 24060
540-552-4610, ext 3801

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

Claim 13 has been amended as follows:

13. (Amended) An etched [micromechanical] **optoelectronic** apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;
b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls
c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls;
d) a patterned metal pad disposed on the dielectric layer;
e) solder disposed on the patterned metal pad.

Claims 19-29 have been added:

19. The apparatus of claim 13 wherein the patterned metal layer includes a U-shaped patterned metal area, and wherein the etched pit is an anisotropically etched pit disposed inside the U-shaped patterned metal area.

20. The apparatus of claim 13 wherein the patterned metal layer includes a ring-shaped patterned metal area, and wherein the etched pit is an anisotropically etched pit disposed inside the ring-shaped patterned metal area.

21. The apparatus of claim 13 further comprising an optoelectronic device soldered to the patterned metal pad.

22. The apparatus of claim 13 wherein the patterned metal pad is spaced away from the dielectric sidewall.

23. The apparatus of claim 13 wherein the patterned metal pad and the patterned metal layer comprise identical deposited materials.

24. An etch d opto lectronic apparatus comprising:

a) a semiconductor substrate having an tched pit with semiconductor sidewalls;

b) a dielectric layer dispos d on the semiconductor substrate, wh rein th diel ctric layer has a hole with diel ctric sid walls, wher in the diel ctric sidewalls are aligned with the semiconductor sid walls
c) a patterned metal layer disposed on th dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls, and wherein the patterned metal layer includes a U-shaped patterned metal area, with the etched pit disposed inside the U-shaped patterned metal area;
d) a patterned metal pad disposed on the dielectric layer;
e) solder disposed on the patterned metal pad.

25. The apparatus of claim 24 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.

26. The apparatus of claim 24 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.

27. An etched optoelectronic apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;
b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls
c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls;
d) a patterned metal pad disposed on the dielectric layer;
e) solder disposed on the patterned metal pad;
f) an optoelectronic device on the solder.

28. The apparatus of claim 27 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.

29. The apparatus of claim 27 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.